ABSTRACT OF THE DISCLOSURE

Each prefetch buffer has a tag register for storing a branch address and a data register for storing instruction data. Each of the prefetch buffers is assigned to either a first prefetch buffer rewritable during a normal operation period and a second prefetch buffer to be disabled for rewrite during the normal operation period. The second prefetch buffer can thus be prevented from being rewritten even if a central processor outputs branch addresses frequently. This realizes an improvement in the instruction fetch efficiency of the central processor and an improvement in the entire system performance. The fetch efficiency can be improved particularly in such systems that branch addresses occur frequently and some of them occur repeatedly.